PATENT ABSTRACTS OF JAPAN

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(54) DELAY CIRCUIT

(57)Abstract:
PURPOSE: To attain minute adjustment of a delay time of a delay circuit and circuit integration by connecting plural capacitors while selecting them as a load static capacitance of an input buffer circuit.
CONSTITUTION: An output of the input buffer circuit 1 is connected to an output buffer circuit 4 and capacitors C1~C4 via transfer gates 11~14. Outputs Q1~Q4 of a decoder 9 are selected by selection signals S(2), S(3). The outputs Q1~Q4 are connected respectively to the transfer gates 11~13, which are tuned on/off. Thus, the capacitors C1~C4 are selected and connected to the output of the input buffer circuit. A desired delay time is obtained by connecting a required capacitor.